TITLE

I/O CIRCUIT PLACEMENT METHOD AND SEMICONDUCTOR DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to an I/O circuit placement method and semiconductor device using the same.

Description of the Related Art

Fig. 1 shows a conventional semiconductor chip having application specific integrated circuits (ASIC). Input/Output buffer circuits 12 (hereinafter referred as I/O circuits) are arranged at the periphery of the chip 10. As shown in Fig. 1, each side of the semiconductor chip 10 has one row of I/O circuits, and the four rows of I/O circuits form a loop.

Conventionally, the I/O circuits in a semiconductor chip are always arranged in one loop around the core circuit 14. Thus, a large number of I/O circuits 12 at the periphery of the chip may enlarge the area of the semiconductor chip 10, and is referred to as the pad limit design. To address this problem, conventional methods have attempted with difficulty to narrow the size of the I/O circuits.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to reduce the space wasted in the pad limit design, thereby reducing costs.

According to the above mentioned objects, the present invention provides an I/O circuit placement method for placing

I/O circuits in a semiconductor device. In the method, at least two rows of I/O circuits are placed on a first side of a chip, and each I/O circuit has a head section and a tail section. The placement direction of the head section and the tail section is perpendicular to that of the I/O circuits in the rows. Further, in the method, the head sections can be oriented to the head sections or tail sections in the adjacent rows. Additionally, different numbers of I/O circuits can be placed in different rows.

According to the above mentioned objects, the present invention provides a semiconductor device. In the semiconductor device, at least two rows of I/O circuits are placed on a first side of the chip, and each I/O circuit has a head section and a tail section. The placement direction of the head and tail sections is perpendicular to the placement direction of I/O circuits in the rows. The semiconductor further has a core circuit disposed on the chip, wherein the rows of I/O circuits are disposed outside the core circuit and at the periphery of the chip.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention can be more fully understood by reading the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Fig. 1 shows I/O circuit placement in a conventional semiconductor chip; and

Fig.2 shows I/O circuit placement in a semiconductor according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 2 shows one example of the layout of the semiconductor device according to the present invention. The semiconductor device includes a semiconductor chip 110 composed of silicon or the like, which includes a core circuit region 140 and a plurality of I/O circuits 120.

In the core circuit region 140, for example, basic cells are arranged in an array such as a gate array. As those basic cells are interconnected via an interconnection layer, an operational circuit with a given function is constructed.

As shown in Fig. 2, the I/O circuits 120 are provided in the outer periphery of the core circuit region 140. In this case, the I/O circuits 120 are arranged in a plurality of rows. Three rows (21, 22 and 23) of I/O circuits are disposed at the left side of the semiconductor chip 100. A row 20 of I/O circuits is disposed on the bottom side of the semiconductor chip 110. Three rows, 24, 25, and 26 of I/O circuits are disposed at the right side of the semiconductor chip 100. Two rows, 27, and 28 of I/O circuits are disposed on the upper side of the semiconductor chip 100. In this case, the rows, 20, 21, 26, and 27 of I/O circuits can form a loop.

In the present invention, each I/O circuit 120 has a head section 121 and a tail section 122. In the row 21, for example, the I/O circuits 120 are arranged in the vertical direction, and the head section 121 and tail section 122 of each I/O cell 120 is arranged in the horizontal direction. Additionally, in row 20, the I/O circuits 120 are arranged in the horizontal direction and the head section 121 and tail section 122 of each I/O cell 120 is arranged in the horizontal direction.

Thus, in the present invention, the placement direction of the head section 121 and the tail section 122 in each I/O circuit 120 is perpendicular to placement direction of the I/O circuits in the rows (20~28).

The tail section 122, for example, can be an input driver, an output driver or an input/output driver to transfer signals to and from the given external device. The head regions 121, each has level shifter circuit to convert signal levels, as interface circuits between the tail section 122 and the basic cells formed in the core circuit region 140. In the case of an external circuit operating at a signal level in the 5V range and the core circuit region 140 operates on a signal level in the 3V range, the head section 121 converts the 5V range signal level from the external circuit to a 3V range signal level or converts the 3V range signal level from the core circuit region 140 to a 5V range signal level.

Moreover, in the present invention, the head sections 121 in the I/O cells 120 can be oriented to the head sections or tail sections 122 in the adjacent rows based on the circuit design. As shown in Fig. 2, for example, the tail sections 122 in the row 22 of I/O circuits are oriented to head sections 121 in the row 21 of I/O circuits, and the tail sections 122 in the row 23 of I/O circuits are oriented to head sections 121 in the row 22. Additionally, the tail sections 122 in the row 24 of I/O circuits are oriented to the tail sections 122 in the row 25 of I/O circuits, and the head sections 121 in the row 25 of I/O circuits are oriented to head sections 121 in the row 26.

As shown in Fig. 2, thirteen I/O circuits are arranged in the rows 20, 26 and 27 respectively, and eight I/O circuits

are arranged in the rows 24, 25 and 28 respectively. Seven I/O circuits are arranged in the rows 22 and 23 respectively, and eleven I/O circuits are arranged in the row 21. In the present invention, the number of I/O circuits placed in different rows can be different according to circuit design. Moreover, the present invention is also applicable to Redistributed Layers (RDL) in flip-chip packages.

As shown in Fig.2, in I/O circuit placement of the present invention, the I/O circuits are arranged in two rows or more at one side of the chip, thus the present invention reduces the space wasted by the pad limit design, and thereby reduces cost.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.